**Claims:**

1. **A method** of forming a process wafer for integrated circuits comprising low voltage and high voltage elements, wherein chip regions (6, 7) of different potential are separated by dielectrically insulating regions (T) by isolation trenches extending from a planar surface (F), at least one of said isolation trenches having or receiving a material that is oxidzable in an oxygen containing atmosphere at an elevated temperature, said method comprising a sequence of main process steps after forming at least two vertical insulating layers (4a, 4b) and a horizontal insulating layer (4a', 4b'):

   - filling said at least one isolation trench with a fill material (5) until a deepest indentation (5c) of a fill material layer (5', 5'') formed on the surface is positioned with its top side above a level defined by the planar surface formed by the insulating layers (4);
   - performing a first planarization process on the fill material layer (5);
   - removing a first portion of the fill material – as a vertical fill layer (5*) – by a first over-removal process down to a defined depth (h7);
   - removing a portion of the insulating layers (4a, 4b, 4a', 4b') and further over-removing of a further portion of the fill layer (5*) so as to obtain or reach a substantially equal height level (h10) of the layers (4; 4a, 4b; 5) within said isolation trench;
   - depositing a cap layer or a layer system as a cover having a thickness extending above the level of the planar surface (F) and extending downwardly to the substantially equal height level within the trench;
   - performing a further planarization process on the cover (9) by a chemical mechanical polishing process or a resist planarization process.

2. The method of claim 1, wherein said cover (9) is an oxygen impermeable cap in the form of a layer system, in particular in the form of a plurality of stacked layers.

3. The method of claim 1, wherein an oxygen impermeable cover (9) is provided as a layer comprised of silicon nitride.

4. The method of claims 1 or 2, wherein said cover (9) is oxygen impermeable and said oxygen impermeable layer comprises at least one layer having a different specific characteristic, such as a specified coefficient of extension or getter capabilities for ions.

5. The method of claim 1, wherein said process wafer is an SOI wafer including a buried insulating layer (2) formed on a carrier layer (1).

6. The method of claim 1, wherein the fill material (4, 5*) of said at least one isolation trench (5a) having said cover (9) is adjusted so as reduce and preferably minimize a bending of the semiconductor wafer.

7. The method of claim 1, wherein the surfaces of the cover (9) and the exposed chip regions (6, 7) define a continuous plane (F) for low voltage and high voltage elements, said plane preferably lacking a step in the trench area and adjacent thereto.

8. The method of claim 1, wherein said insulating layers (4; 4a, 4b, 4a', 4b') are formed by a thermal oxidation.

9. The method of claim 1, wherein said fill material (5; 5', 5'', 5*) is polysilicon.

10. The method of claim 1m wherein the concurrent removal of the insulating layers (4a, 4b, 4a', 4b') and the vertical fill layer (5*) is performed with a defined measure of depth removal by an etch process, preferably across the entire trench width.

11. The method of claim 1, wherein only a mask for forming said at least one trench (5a) is used for the process steps of claim 1.

12. The method of claim 1, wherein the first and the second removal of the fill material (5*) located within the trench are defined etch-back processes.

13. The method of claim 1, wherein said cover (9) lowered into said trench forms a vertically or laterally acting insulation across an entire trench width (9b).

14. The method of claim 1, wherein said cover (9) is dielectrically insulating.

15. The method of claim 1, wherein said low voltage elements are logic elements.

15. The method of claims 1 or 15, wherein said high voltage elements are power elements.

17. The method of claim 1, wherein the elements are located or are formed in an active semiconductor layer (3).

18. The method of claims 1 or 17, wherein said active semiconductor layer (3) extends horizontally and is bordered in the vertical direction by a buried insulating layer (2).

19. The method of claim 1, wherein at least one isolation trench (T, 5a) is formed in an active semiconductor layer (3) to a lower end thereof at a buried insulating layer (2).

20. The method of claim 1, wherein said fill material (5*) is electrically conductive, in particular is a polysilicon, or is (slightly) oxidizable.

21. The method of claims 1, wherein during the first removal (over-removal) of the fill material within said isolation trench (5a) the removal isperformed not deeper (h7) than down to half of the trench depth, in particular to approximately ¼ of the trench depth or less.

22. The method of claims 1 or 21, wherein during the further removal (over-removal) material is removed not deeper (h9) than down to half of the trench depth, in particular to approximately ¼ of the trench depth or less.

23. The method of claim 1, wherein said trench depth (h0) in the active semiconductor layer (3) is greater than 1µm, in particular greater than 10µm or is substantially 50µm.

24. The method of claims 1 or 23, wherein said at least one isolation trench (5a) has an aspect ratio of depth to width that is higher than 10:1, and in particular higher than 15:1.

25. The method of claims 1 or 19, wherein said vertical insulating layers (4a, 4b) at both trench walls are or have been formed down to the horizontal insulating layer (2), when said main process steps start.

26. **A process wafer** (1, 2, 3) formed or formable according to any of the preceding method claims.

27. **A method** for treating an SOI wafer (1, 2, 3) and forming therein dielectrically insulating isolation trenches (5a, T) between two regions (6, 7) of the active semiconductor layer of the SOI wafer, said regions being associated with respective two different potentials (P1, P2), said method comprising: forming insulating layers (4a, 4b) laterally on walls of a formed trench structure (5a), filling a gap in the trench with a fill layer (5*), removing the fill layer (5*) down to a certain trench depth (h9, h7) together with a portion of the lateral wall insulation (4a, 4b) so as to obtain a substantially equal height level (h10) of the upper ends of the three layers being present in said trench, and depositing a cap layer (9) at least on the upper ends and in the vicinity of the active semiconductor layer (3) including a removal (planarization) of said cap layer down to a laterally extending planar surface (F) above the filled trench and at least within the neighbouring area at both trench sides so as to expose said semiconductor layer (3) adjacent to the respective insulation trench.

28. **An at least partially processed SOI wafer** for further processing comprising a trench structure (T) including within the trench an insulating layer sequence of vertically oriented first layers (%+, 4a, 4b) that are covered at the top side by a second layer (9) laterally extending to and on the walls of the trench, thereby forming a planar surface (F) of the SOI wafer, two of said first layers (4a, 4b) extending down to a buried insulating layer (2) of the SOI wafer.

29. The method of claims 1 or 11, wherein said cover (9) is formed without a mask.

30. ...

31. **A method** of forming electric circuits, said electric circuits having integrated therein low voltage logic elements and high voltage power elements, the chip regions of different potential being separated from one another by dielectrically insulating regions by isolation trenches extending from the planar surface and including materials capable of oxidizing at elevated temperatures in an oxygen containing atmosphere, said method being **characterized by** a sequence of the following main processes after forming the insulating layers (4):

- filling said isolation trench with a fill material (5) until the deepest indentation of the fill material layer is positioned at its top side above the level of the planar surface defined by the oxide layer (4);
- planarizing the fill material (5);

- removing said fill material in the trench to a defined depth by over-etching;
- etching said oxide layers (4) and over-etching said fill material (5) so as to obtain a substantially equal height level of the layers (4) and (5) within the isolation trench;
- depositing the cap layer (9) or a layer system with a thickness that extends above the level of the planar surface;
- planarizing said cap layer or said layer system by chemical mechanical polishing or by performing a resist planarization process.

32. The method of claim 31, **characterized in that** the oxygen impermeable cap layer is a layer system, i.e., is comprised of a plurality of stacked layers, wherein said oxygen impermeable layer is combined with layers of other specific characteristics, such as specific coefficients of expansion and getter capabilities for ions.

33. The method of claim 31, **characterized in that** the oxygen impermeable cap layer is layer comprised of silicon nitride.

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